Remarks

Claims 1-7, 9, 10, 12-15, and 18-24 have been rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,313,624 (Harriman *et al.*), hereinafter "Harriman". Applicants respectfully disagree.

The present invention comprises a system and method for handling data for data processing means utilizing a plurality of memory registers. A first and second multiplexor means, each coupled to the memory registers, receives and outputs data from, and to, the processing means, respectively. The plurality of registers is configured into slices of arrays. Each slice has two (multiple) independent inputs coupled to the first multiplexor means, and two (multiple) independent outputs coupled to the second multiplexor means. The identification and location of data being stored to the registers from the first multiplexor means are tracked, and the identified data for output to the second multiplexor means are selected.

The present invention also provides a system wherein the multiplexor continuously selects the memory registers sequentially, and sequentially stores the data from the multiplexor beginning at any data storage line within any of the memory slices. The system of the present invention therefore, provides a multiplexing function that allows the distribution of data to several different memory arrays with continuous data flow.

Harriman does not disclose such a system. As Applicants stated in the Description Of The Related Art section of the present application, Harriman simply discloses "the use of a multiplexor to route data to one of four memory arrays. Page 3, lines 20 – 22. Contrary to the Examiner's findings, the CPU registers 307A – 307D, illustrated in Fig. 3, do not have two independent inputs coupled to the first multiplexor, nor do they have two outputs coupled to the second multiplexor. In fact, as clearly illustrated in Fig. 4, CPU registers 307A – 307D are not coupled to the second multiplexor at all. (See, Fig. 4 and Col. 10, lines 37 –68).

Also, Fig 4 of Harriman clearly illustrates that each one of the first multiplexors (306A – 306D) is coupled to a corresponding register (307A – 307D). Unlike Harriman, the present invention comprises a plurality of registers configured into slices, wherein all slices of arrays are coupled to the first multiplexor.

As such, the means to track the identification and location of data being stored to the registers, and the means to select identified data within the registers for output to the second

multiplexor means, claimed in the present invention, are not "embedded in [Harriman]", which is contrary to the Examiner's finding in the Detailed Action. Detailed Action, page 3. As it is understood by the Applicants, since the Harriman system simply couples the first multiplexor to one of four registers, Harriman simply stores and the reads the data from the first register associated with the first multiplexor coupled thereto, and steps through the remaining registers and multiplexors in sequential order, always beginning at the first register. This is clearly set forth in col. 7, line 37 – col. 9, line 20 of Harriman. Contrary to Harriman, as stated above, the multiplexor of the present invention continuously selects the memory registers sequentially, and sequentially stores the data from the multiplexor beginning at any data storage line within any of the memory slices. Harriman does not disclose such a system. Therefore, as stated above, the means to track the identification and location of data being stored to the registers and the means to select identified data within the registers for output to the second multiplexor means can not be inherently taught by Harriman. Simply put, as it understood by the Applicants, Harriman does not teach the same architecture that the present invention teaches.

Accordingly, Harriman does not and cannot anticipate the system as claimed in pending claims 1 – 24, because such anticipation would require each and every step of the present invention to be taught by the cited reference, which Harriman fails to do. Therefore, it is respectfully submitted that claims 1 – 24 are patentable over Harriman.

Similarly, even if combined with other prior art, including the prior art made of record and not relied upon, Harriman could not provide a basis for an obviousness rejection of the present invention. The steps missing in Harriman that distinguish it from the present invention cannot be added by additional art to combine to teach Applicants' system and method for handling data for data processing.

It is respectfully submitted that claims 1 - 24 are in condition for allowance. Applicants respectfully request that allowance be granted at the earliest date possible. Should the Examiner have any questions or comments regarding Applicant's amendments or response, the Examiner is asked to contact Applicant's undersigned representative at (215) 575-7194.

In the event any additional fees are required in connection with this paper, please charge Deposit Account No.: 50-0979.

Respectfully submitted,

Darryl W. Shorter
Registration No. 47,942

Date: **February 10, 2004**

DILWORTH PAXSON LLP
3200 Mellon Bank Center
1735 Market Street
Philadelphia, PA 19103-7595
Tel. (215) 575-7000
Fax (215) 575-7200

516425_1